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Abstract

The present invention provides a method for fabricating a semiconductor structure having the steps of: providing a semiconductor substrate (10); providing a plurality of trenches (G11, G12; G21) in the semiconductor substrate (10) using a first hard mask (50), which trenches are arranged offset with respect to one another in rows (r1, r2) and columns (s1, s2, s3); causing the hard mask (50) to recede by a predetermined distance (Δ) with respect to the trench wall at the top side (OS) of the semiconductor substrate (10) for the purpose of forming a first hard mask (50') that has been caused to recede; providing an isolation trench structure (ST) in the semiconductor substrate (10) using a second hard mask (HM), the isolation trench structure (ST) subdividing the first first [sic] hard mask (50') that has been caused to recede along the rows (r1, r2) into strip sections (50_1', 50_2'; 50_3') and the strip sections (50_1'; 50_3') of adjacent rows (r1, r2) being arranged offset with respect to one another; the receding process resulting in a reduction of an overlap region (KB') between two strip sections (50_1'; 50_3') of adjacent rows (r1, r2) in comparison with an overlap region (KB) which would be present without the receding process; removing the second hard mask (HM); and filling and planarizing the isolation trench structure (ST) with a filling material (FI) using the first hard mask (50') subdivided into the strip sections (50_1', 50_2'; 50_3').

Figure 1e

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List of reference symbols

G1-G8	Trench capacitors
AA1-7	Active regions
STI	Shallow trench isolation
r1, r2	Rows
s1, s2, s3	Columns
10	Si semiconductor substrate
20	Polysilicon filling
OS	Top side
G11, G12, G21	Trench
UC	Undercut region
V	Connecting line
Δ	Receding distance
50, 50'	Silicon nitride hard mask
HM	Hard mask made of silicon oxide
ST	Isolation trench structure
$50_1'$, $50_2'$, $50_3'$	Strip sections
FI	Insulating filling material made of silicon oxide
KB	Overlap region
KB'	Reduced overlap region